DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 2003/0143772).

Regarding claim 5, Chen discloses a method for manufacturing a compound semiconductor substrate, comprising the steps of: (f) epitaxilaly growing a compound semiconductor functional layer (Fig.6A, numerals 102-119) on a substrate (Fig.6A, numeral 100), (g) bonding a thermally conductive substrate (Fig.6B, numeral 125; Fig.6C) having a thermal conductivity higher than that of the substrate (Fig.6A, numeral 118)) to the surface of the compound semiconductor functional layer ([0028]) and (h) polishing the substrate and a part of the compound semiconductor functional layer on the side which is in contact with the substrate to remove them ([0030]).

Regarding claim 6 Chen discloses the compound semiconductor functional layer includes at least two layers (Fig.6A).

Regarding claim 7, Chen discloses that the compound semiconductor functional layer includes at least one selected from the group consisting of In, Ga, and Al and at least one selected from the group consisting of N, P, and As [0023]-[0025]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (JP 6-349731) in view of Ravi (US 2004/0191534).

Regarding claim 1, Mori discloses epitaxilaly growing a compound semiconductor functional layer (Fig.4a, numerals 21,32,6,3), on a substrate (Fig.4a, numeral 4); bonding a support substrate (Fig.4c, numeral 41) to the compound semiconductor layer (paragraph [0058]); polishing the substrate and a part of the compound functional semiconductor layer on the side which is in contact with the substrate, to remove them (Fig.4c; paragraph [0058])); bonding a thermally conductive substrate (Fig.4D, numeral 1, paragraph [0059]) having a thermal conductivity higher than that of substrate (4) (note: substrate (4) is InP, [0054], and substrate (1) is Si) to the exposed surface of the compound semiconductor functional layer (3) to obtain a multilayer substrate and separating the support substrate (41) from the multilayer substrate (Fig.4e, [0060]).

Mori does not disclose that (1) the thermally conductive substrate includes a substrate formed diamond thin film having a thickness of about not more than 300 μm and about not less than 50 μm on a single crystal Si substrate, polycrystalline Si substrate or ceramics substrate and (2) that the diamond film is a polycrystalline or amorphous.

Regarding element (1), Mori discloses that the thermally conductive substrate is a Si substrate ([0002]). And Ravi discloses using a support substrate forming with a diamond thin film having a thickness of 100 mm (Fig. 2C, numeral 214; [0022]; [0025]) on a polycrystalline Si substrate (Fig.2C, numeral 205, [0019]) for the purpose of spreading heat away form active devices of an integrated circuit ([0016]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Mori with Ravi to have the thermally conductive substrate includes a substrate formed diamond thin film having a thickness of about 100 μm on a polycrystalline Si substrate for the purpose of spreading heat away form active devices of an integrated circuit (Ravi, [0016]).

Regarding element (2), Ravi discloses that the diamond film is formed by CVD ([0022]). And forming a polycrystalline or amorphous film is a typical result of using CVD process.

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to have a diamond film as a polycrystalline or amorphous film since it is typical results of using CVD process.

Regarding claim 2, Mori discloses that the compound semiconductor functions layer includes at least two layers (Fig.4a, 21, 32, 6, 3).

Regarding claim 3, Mori discloses that the compound semiconductor functional layer includes at least one selected form the group consisting of In, Ga and at least one selected form the croup consisting of N and As [0054]).

Regarding claim 9, Mori does not disclose a step of forming an electrode on the resultant compound semiconductor device.

It would have been however obvious to one of ordinary skill in the art at time the invention was made to form an electrode on the resultant compound semiconductor devices for the purpose of using this structure as a light emitting diode.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied to claim 5 above, and further in view of Ravi.

Regarding claim 10, Chen discloses all limitations of claim 5 for reasons above. Chen does not disclose that (1) the thermally conductive substrate includes a substrate formed diamond thin film having a thickness of about not more than 300 μm and about not less than 50 μm on a single crystal Si substrate, polycrystalline Si substrate or ceramics substrate and (2) that the diamond film is a polycrystalline or amorphous.

Regarding element (1), Ravi discloses using a support substrate forming with a diamond thin film having a thickness of 100 mm (Fig. 2C, numeral 214; [0022]; [0025]) on a polycrystalline Si substrate (Fig.2C, numeral 205, [0019]) for the purpose of spreading heat away form active devices of an integrated circuit ([0016]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Chen with Ravi to have the thermally conductive substrate includes a substrate formed diamond thin film having a thickness of about 100 μm on a polycrystalline Si substrate for the purpose of spreading heat away form active devices of an integrated circuit (Ravi, [0016]).

Regarding element (2), Ravi discloses that the diamond film is formed by CVD ([0022]). And forming a polycrystalline or amorphous film is a typical result of using CVD process.

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to have a diamond film as a polycrystalline or amorphous film since it is typical results of using CVD process.

6. Claims 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Ravi as applied to claim 1 above, and further in view of Hsieh (US 2005/0074927).

Regarding claim 11, Mori in view of Ravi discloses all limitations of claim 1 for reasons above.

Mori does not disclose that the bonding step is performed by using an adhesive such that the support substrate may be removed from the compound semiconductor functional layer without providing chemical and physical damage on the epitaxial growth surface of the compound semiconductor functional layer.

Hsieh however discloses using an adhesive in the substrate bonding using an adhesive for the purpose of minimizing thermal damage to the template ([0085]). Examiner also would like to note that the limitation "such that the support substrate may be removed from the compound semiconductor functional layer without providing chemical and physical damage on the epitaxial growth surface of the compound semiconductor functional layer" is an intended outcome recitation of the positively

recited step of "using an adhesive" rather then required step further limiting the scope of claims. Since Hsieh discloses "using an adhesive," it anticipates this limitation.

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Mori with Hsieh to perform the bonding by using an adhesive such that the support substrate may be removed from the compound semiconductor functional layer without providing chemical and physical damage on the epitaxial growth surface of the compound semiconductor functional layer for the purpose of minimizing thermal damage to the template (Hsieh, [0085]).

Regarding claim 12, Hsieh discloses that the adhesive is an adhesive tape (Fig.17, [0089], [0090]).

Response to Arguments

7. Applicant's arguments filed 03/09/2010 have been fully considered but they are not persuasive.

8. Applicant's arguments that Chen does not disclose "(f) epitaxilaly growing a compound semiconductor functional layer... (g) bonding a thermally conductive substrate ... to the surface of the compound semiconductor functional layer (22)" as recited in claim 5 are not persuasive since Chen discloses (f) epitaxilaly growing a compound semiconductor functional layer (Fig.6A, numerals 102-119) on a substrate (Fig.6A, numeral 100), (g) bonding a thermally conductive substrate (Fig.6B, numeral 125; Fig.6C) having a thermal conductivity higher than that of the substrate (Fig.6A, numeral 118)) to the surface of the compound semiconductor functional layer ([0028]).

9. Applicant's arguments with respect to claims 5-7 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
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/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
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